Wiring the Camera

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Executive Summary

Active components will be required in the dewar to meet the proposed read out rate. These are proposed to be located on a small circuit board where the cable connects to the connector on the AlN substrate. Several possible configurations are discussed

Two RTMA rack sized crates are required each containing two MONSOON CompactPCI backplanes. An alternative would be to mount the four CompactPCI backplanes separately.

Introduction

This note will investigate the wiring of the camera. This is very preliminary since the information needed is not yet available. In particular, the connections to the CCD are not yet understood. The proposed pin connections are thus an educated guess. It is also tedious in some detail. As Ross Perot would say, "The Devil is in the Details". It is difficult to be rational about a complicated system without pointing at the detail that causes a problem.

There are several problems that beg for early attention. Fermilab has great experience in the design of large precision mechanical structures, vacuum systems and large scale computation. It is understandable that the mechanical designers are champing at the bit to start work on their view of the problems of this camera. One of the purposes of this note is to establish a likely electronic configuration so that the mechanical designers can start work.

The problems related to the precision measurement of large numbers of analog channels at high speed are of similar difficulty to the problems of building the mechanical structure. The desired read out rate of 240 KHz is beyond the speed at which LBNL literature says the device will operate. There is surely an increase in noise due to the shorter integration times associated with the faster read out rate. The design report indicates that noise might be sacrificed for speed. There is limited CCD design experience represented by staff at the group meetings. It is recommended that a path be planned that gets the required experience as quickly as possible. There is a speed – noise trade off to be determined. Good decisions as to the wiring configuration cannot be made until there is a better understanding of the CCD characteristics. It would not appear that it will be easy to transfer experience to Fermilab from LBNL. The only likely way to get the necessary experience to do the design is by hands on operation of CCDs here at Fermilab. This is a critical path that is at least as long as that of the optical design. One cannot make good electronic design decisions until one is experienced in operating the CCD devices. This takes time.

We are working energetically on a test dewar design which will allow taking scientific measurements on these devices at their final operating temperature. The fabrication of this device is apt to take some time. We cannot afford to wait to start getting working experience with these devices until such a test dewar is ready. Many things can be learned at room temperature or at a cool temperature in the dark. Such a test fixture can be assembled out of string, glue and Styrofoam. This author recently constructed a facility in about two weeks with an 8 hour a week helper. Some of the TASS electronics could be acquired to operate such a facility if Monsoon crates cannot be acquired quickly. Note that Monsoon is fundamentally a large system. It may take some time to turn it on and get all the software working. This is apt to focus attention on developing the digital and computer aspects of Monsoon rather than the analog design problems which are advised to be more on the critical path.

What is the worry? It is not clear that the 240KHz read out rate can be met at an acceptable noise level. Alternatives are to, for example, read out the chip from 4 corners. This requires a new mask design, double the cables, double the Monsoon crates, and double the connectors through the dewar wall. This would throw out most of the mechanical work that might have been done by the time this is discovered to be a problem.

CCD samples should thus be acquired and operating experience should be gained as quickly as possible.

An example of some of the work that needs to be done is that the capacitance of the clock lines needs to be known in order to design drivers. A rough estimate indicates that there might be a meter between the driver circuit on a MONSOON card and the clock line on the CCD. It is doubtful that clock lines can be driven over this distance. A measurement needs to me made. Circuits need to be tested. A test fixture is needed to start this work.

As questions are asked, it is found that the answers come slowly if at all. This is understandable. Those at other laboratories have other projects. A tough question requires work to answer. We will have problems that do not exist at other laboratories. Building a big detector is a lot different work than developing devices. We will have to build test fixtures that allow us to get answers to engineering questions. This is a critical path.

Ground

When this note was started, it seemed appropriate to change the name of what is usually called "High Quality Ground" or AGND in the MONSOON specification to "Zero Voltage Reference" to emphasize that AGND is not the same value everywhere. This now seems a bit extreme. The concept is still valid. There is no place in a large system that you can count on not being a different potential from it's same name in another place. AGND just does not exit to the accuracy of the conversion process which is of order 10uv per least significant bit in a system that is being constantly switched.

Following the MONSOON specifications as closely as possible, there are at least 3 "Grounds" to be considered. These are AGND, GND, and CHASSIS.

It is proposed to keep these grounds separate. Eventually they will be connected together at one point, but that point should be well identified and should allow separation to search for ground noise problems.

In general there will be a different AGND for each signal. When a signal is moved anywhere, it's AGND is taken with it. This is emphasized by labeling the AGND for signal n as AGND(n).

Possibly this is preaching to the "Choir." If so that is just fine and no one will resist the wiring scheme that is proposed here. The Choir may have ideas as to how to do it better. That would be great. The goal here is to think carefully about moving signals from place to place at the beginning of the project. Then possibly there will be no noise problems to solve at the end.

CCD Packaging

The package that has recently been discussed is assumed. Figure 1a and b. The CCD is glued to an AlN backing circuit board and is wire bonded to it. A connector is fastened to the AlN board. The connector sits in a well in the precision foot that is glued to the AlN substrate. The mating connector is fastened to a small circuit board. At the end of the circuit board a flexible cable transports the signals to the connectors in the dewar wall.

In keeping with the separation of grounds plan, the precision mounting block is insulated from the AGND and is connected to a wire brought out through the AlN connector. If this is im-

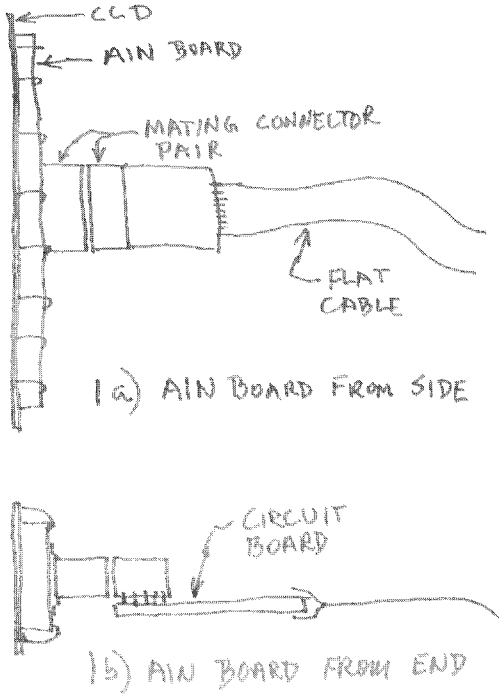

Figure 1. Location of Cable Card Circuit Board

possible to achieve, the alternate plan is to put a large ground plane under the precision mounting block and bring out a connection to it. .

CCD Wiring

The first problem is to decide on what should be done on the AlN board. It is assumed that after this board is processed so that the surface behind the CCD will need to be lapped flat. This precludes any wiring on that side. It would be preferable to have a ground plane there. It is assumed that the AlN board can be multi-layered on the side away from the CCD. The design can make do with a ground plane on this side. This board can be wired to it's connector so that there are no limitations as to what can be done with the CCD. By wiring on the AlN board, the connector pin count can be reduced. This can be at various levels with reduction of flexibility as pin count is reduced.

A1

No wiring is done on the AlN board. A 37 pin connector is used which matches the LBNL pin out. This makes the CCD compatible with LBNL test stations. There are 3 spare pins on the LBNL layout. These can be used for an RTD with the return excitation lead using one of the P+ pins with is assumed to be athe AGND pin. This should retain compatibility with LBNL test fixtures while allowing wiring on the Cable Card to keep the RTD separate for the A2 and higher configurations.

A2

With this version we eliminate frame store which is not planned to be used. It assumes that the chip will behave the same way for RG, SW, and TG so these can be adjusted together for the two chip sides. Vdd pins are brought out for each amplifier so that there can be a separate protection circuit for each output allowing the setting of tighter protection limits and of turning of one amplifier at a time. The pins are numbered to keep count. Later the best pin arrangement will be chosen. Without the RTD his gets the pin count below 25 pins which is the next smaller Nanonics connector from the 37 pin connector used by LBNL. With the RTD it will fit the 37 pin Nanonics connector with spares.

1 Vsub
2 p+ bring at least two through the connector. Probably 1 on each end
3 H1 U bring out all the horizontal clocks to allow all possible clocking combinations
4 H2 U
5 H3 U
6 Vr U
7 RG U/L
8 Video U
9 Vdd U
10 V opg U
11 SW U/L
12 TG U/L
13 p+
14 FS1/V1 tied together gives up frame store
15 FS2/V2
16 FS3/V3
17 n+ guard
18 H1 L
19 H2 L
20 H3 L
21 Video L

22 Vdd L
23 Vopg L
24 Vr L
25 RTD
26 RTD
27 RTD
28 RTD

A3

It is possible to reduce the pin count further if we discover through testing that other signals can be combined. Since it is unlikely that any combination will get to the next connector size around 15 pins there is little incentive.

Cable Card

A small surface mount or wire bonded board is envisioned. Several possibilities are considered for active components in the dewar. This adds complexity and puts stuff in the dewar where it will be hard to fix. There is a compelling reason. The system has been specified to read out at a 240 Kpixel rate. This is beyond the rate that is implied for lowest noise by the LBNL data. The wiring distance from the back plane of the MONSOON system to the AlN substrate is of order a meter. It would appear to be difficult to drive clocks over a meter of cable. It is just a question of rate. The system can probably be made to work at some rate over a meter of cable, but this is not even certain since there might be so much clock bounce that the charge is not properly transferred without careful shaping of the clock edges.

The possible rate is being pushed, so the very best clocking technique is advised. This requires active components near the CCD. The best place for these parts would be on the AlN substrate. This real estate is very valuable for other purposes. We thus propose a small circuit board either as the mating connector mounting spot as shown in Figure 1, or in a flexible cable close to the connector. By close, a few cm is indicated.

With careful design, the parts count can be kept to 40 or so for the clock designs like B4 below with possibly 50 parts needed for the design with a preamplifier. This should fit on both sides of a 1" x 1" board for B4 and a little larger for B5 using surface mount techniques if these do not pose a vacuum problem. Otherwise chips can be wire bonded.

Putting the clock driver on the Cable Card requires more wires. This is because it requires both a logic signal and two clock levels to generate a local clock as in Figure 2. Since many of the voltages are the same, only about 6 additiona wires are needed bring the total wires in the cable coming off the back of the cable card to 34.

B1

This configuration has no circuit board. The AlN connector is wired straight through with all 37 pins wired to a connector in the dewar wall.

B2

Clock DC levels and logical clock signals are wired to the Cable Card where the actual clocks are generated with SPDT solid state switches. This is done for only the horizontal registers which must clock the fastest. A schematic is shown as Figure 2.

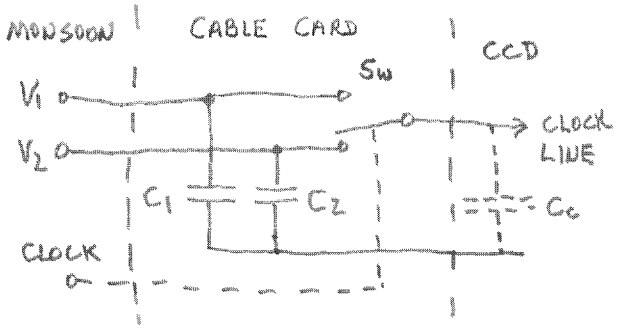

Figure 2. Basic Clock Drive Circuit

Common practice is to put a series resistor in the clock line and to put a capacitor to AGND at the clock terminal. Good understanding of the clock capacitance, proper conductor routing, and proper switch selection should allow dispensing with these extra parts.

Capacitors on the Cable Board provide most of the transient switching charge. DC clock current is due to the amount of charge needed to make a clock transition x the number of charge transitions during read out divided by the read out time. This is roughly (3 clocks x 10 volt transition x 100 pf clock line capacitance x 2000 horizontal clocks x 4000 vertical clocks)/16 seconds. This is an average current per CCD of 1.5 ma or 90 ma for the camera during readout. This is quite manageable. The peak current depends on the switch used. If we assume 100 ohms and a 10 volt transition, then the peak current is 100 ma per CCD and 6 amperes for the camera. This is a large enough current to cause a lot of ringing in the camera structure if it is attempted to be transmitted over the 1 meter cable. The purpose of the local clock drive switches is to attempt to confine the high switch currents to the locale of the CCD. If these currents are propagated through the whole dewar volume they would be expected to couple into the CCD video output and would cause a loss of accuracy. How much? There is no way to tell without modeling the exact cable configuration. Even then a small cable change could result in a big error. It is recommended that the best way to eliminate this problem is to reduce the transient currents in the dewar.

B3

This is the same as B2 except that switches are added for the vertical clocks.

The vertical clocks have roughly 2000 times the capacitance as the horizontal clocks (if I have the geometry right) however the peak current is the same. Further since there are fewer, the average current is about the same. The peak current is limited by the impedance that drives the clock line. Either the cable if driven from outside the dewar or the switch resistance if driven from a circuit on the cable board. The vertical clocks are probably a lessor problem than the horizontal clocks even though they are much higher in capacitance. Further, if there is a problem in driving them, it is possible to allow significant settling time at small cost in read out time. Adding 10 microseconds to each vertical clock transition for settling might add only 0.2 seconds to the read out time. Adding the same amount of time to the horizontal clocks would increase the read out time by 400 seconds. One might need a similar time for each clock edge for each transition for best accuracy. Not that the settling times are understood. This only to point at the problem. The horizontal clocks are the problem even though they are the lower capacitance drive.

B4

Protection circuits are added on the Cable Board with this version. Sample protection circuits are shown in Figure 3 which also explores how the video signal might be transmitted to the MONSOON system.

Cg represents the charge storage well in the CCD. The reset pulse sets the charge level in this capacitance. This voltage level is buffered by the output transistor which drives the signal over

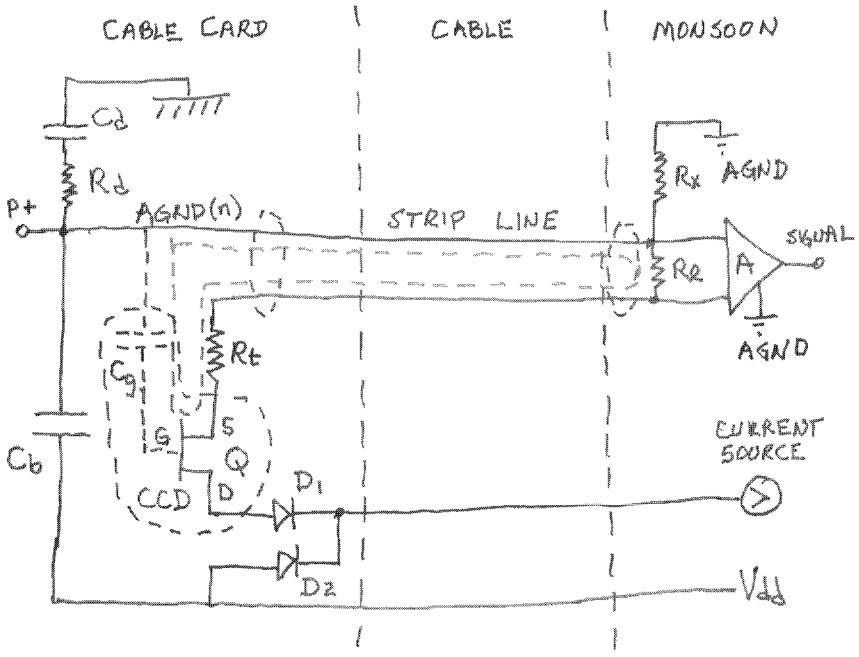

Figure 3. Video output transmission and protection.

the strip line to the MONSOON system crate where it is received by a fast instrumentation amplifier (A). This amplifier is selected to have good common mode rejection over wide bandwidth. The AGND (n) for this signal is carried with it over the strip line. The (n) in the AGND designation indicates that we do not expect the AGND to have the same value everywhere in the system. In red we show the critical path for this signal. The Cg capacitor is referenced to AGND(n) and the video transistor drives against this ground. This assumes that the video transistor has a stiff drain supply that is also referenced to AGND. After the clock transfers the pixel charge to Cg, the video amplifier drives the cable with a step through Rt. Rt with the output impedance of the video transistor is designed to terminate the impedance of the strip line. This is always far from perfect. However, the strip line is only a meter or so long so the time for a few bounces is reasonable. The output current spike is provided by current switching from D2 to D1.

To protect the output transistor from burn out (it is easily done) some protection circuitry is included. The transistor supply voltage is set by Vdd. The available current to the video output transistor is set by the current source. This is set to be somewhat greater than the current required by the load, and somewhat less than that which will result in the destruction of the video output transistor. The needed load current flows through D1 from the current source. Any excess current from the current source is clamped through D2 to the Vdd supply. If the currents through D1 and D2 are set to be nearly equal, then the voltage drop across D1 and D2 will be equal and the drain voltage of the video transistor can be set by Vdd. This scheme is shown since it is very simple. Other schemes are possible.

The impedance of the video amplifier Vdd supply is determined by the forward biased impedance of the two diodes in series. This is low compared to the load resistance of the video aomplifier. The Vdd power is bypassed to AGND(n) by Cb so that the video will have high speed drive capability up to the current limit set by the current source.

The purpose of Rx is to set the bias levels of the clocks otherwise AGND(n) could float. The smaller the value of Rx the more the common mode rejection of the instrumentation is reduced. The real circuit is much more complicated than Figure 3 when all the parisitics are considered. Rx is also one of the damping elements which takes energy out of a ringing structure.

With any of the schemes which generate clocks in the dewar B3 – B5, the length of wire is no longer critical between the MONSOON crates and the dewar. With B4 and B5 one might successfully go 5 meters. For lightning protection reasons, it is not recommended to put the MONSOON crates outside a shield enclosure. However, once the clocks are generated in the dewar, the cables can be dressed for ease of routing and maintenance both inside and outside the dewar.

B5

A preamplifier is added on the Cable Card. There may be noise problems with the circuit of B4. In this case, it may be desirable to put a pre-amplifier on the Cable Card. This has the added advantage that it protects the video output amplifier from damage. It has the disadvantage of putting additional power into the dewar. This might be of order 50 mw per amplifier or 5W for the system.

Dewar Wiring

C1

Minimal wiring in the dewar. Wires from the AlN connector are wired pin to pin to connectors in the dewar wall.

C2

Cable cards increase the number of wires brought out but there is still one connector for each CCD chip. The small increase over the minimum possible number of wires allows higher speed clocking.

C3

Clocks are distributed inside the dewar. This greatly (about a factor of two) reduces the number of connections brought through the dewar wall. This has two bad effects. It requires split cables connecting to the Cable Card, and it actually increases significantly the number of connector pins required in the system.

Monsoon Wiring

The MONSOON standard provides a convenient place to do the necessary wiring for any of the schemes discussed. This is done with special analog backplanes and the "personality" cards that are plugged into the back of the crate.

Dampers

The dewar structure is large and will ring every time there is a clock transition. The plan is to compensate for the ringing in two ways. Each video signal is carried differentially to an instrumentation amplifier at the MONSOON crate. This reduces the sensitivity to any ringing that occurs. Damping networks are planned throughout the structure to remove energy from the system.

Solutions

As indicated by the lists above there are many possible configurations for the wiring. Several are discussed.

Simplest A1B1C1

The simplest solution is to wire each AIN card straight through to the MONSOON system where wiring is routed through the special analog backplane as required. Possibly this will function at some speed. Possibly it will not work at any speed due to clock bounce. Possibly it will even work at the desired speed. It is chancy enough that it would be recommended that a complete model of the wiring be built to test for noise with a sample chip.

Fastest A2B5C2

This is the same as the recommended plan below with the addition of a preamplifier. Pre-amplifiers should reduce the probability of a noise problem, but add about 5 watts in the dewar.

Smallest Dewar Pin Count A2BnC3

In this scheme clocks and bias voltages are distributed inside the dewar. This cuts the dewar wall pin count in half, but requires split cables and even more connections inside the dewar are eliminated. This is not recommended unless dewar wall connections prove expensive and difficult.

Recommended A2B4C2

The recommended scheme puts the clock drivers on the Cable Card near the CCD. DC voltages for the clock levels are wired into the Cable Card where logic level controlled switches generate the clocks. This scheme generates the lowest possible switch noise in the dewar. Each CCD is wired to it's individual connector. The video output is driven over strip line to the MONSOON crate where it is received by a fast instrumentation amplifier.

Over All Plan

So far the only information about the available cards is that there is a Clock and Bias board with 32 available clocks and 36 bias supplies, all with a a range of +/- 15 volts. There is an 8 channel ADC board with also has 32 +/- 40 volt bias supplies. Schematics are really needed to check on drive capacities, etc..

The general plan is to divide the camera into four quadrants. One MONSOON backplane controls each quadrant. Assuming 64 CCDs there will be 16 per quadrant with a few additional required for the focus and guide chips. These can be allocated to spare slots.

For a quadrant, there are 32 output amplifiers. Each takes an ADC channel. Using the circuit of Figure 3, each also take two of the 40 volt bias voltages that are available on the ADC board. One for Vdd and one for the current source. One of the 40 volt supplies might be used for Vsub. This may not allow a high enough voltage. If not, it will be boosted on the personality board on the crate back.

If we plug 4 ADC cards and one Clock Bias board in a crate we have available:
32 ADC channels
128 40 volt bias supplies
32 clocks
36 low voltage bias supplies.

Each ADC channel needs:
1 ADC Channel
3 40 volt bias channels
2 low voltage bias channels

9 Clocks are needed which *must* be common to all circuits except for the guide CCDs which cannot be clocked during the science camera read out. The available channels can be split to provide necessary fan our, or driver circuits can be put on the personality board since the preferred scheme uses logic level clocks.

The preferred scheme uses per quadrant:
32 out of 32 available ADC channels.
24 out of 128 available 40 volt bias channels
9 out of 32 available clocks
16 out of 26 low voltage bias supplies.

By adding an ADC board in one (or two compact PCI crates for symmetry), the guide and focus chips beyond 64 can be accommodated.

We will need to design a card to read the RTDs. The same card might also drive the heaters. We might need two of these cards. This scheme uses 28 out of the 32 card slots available in 4 CompactPCI crates. There are plenty of extra clock and bias channels in case the needs have been miscounted.

Total card count for the system:
4 CompactPCI Backplanes
18 ADC Cards
4 Clock Bias Boards
2 RTD boards
4 System Boards
4 Spare Card Slots